



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/608,869	06/30/2000	Stephen S. Chang	042390.P8815	2389

7590

11/20/2003

Blakely Sokoloff Taylor & Zafman LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025

EXAMINER

BANANKHAH, MAJID A

ART UNIT

PAPER NUMBER

2127

DATE MAILED: 11/20/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/608,869

Applicant(s)

CHANG, STEPHEN S.

Examiner

Majid A Banankhah

Art Unit

2127

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 August 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

Art Unit: 2127

1. This office action in response to application filed on August 18, 2000. Applicant argument has been fully considered but they are deemed to be moot in view of the new ground of rejection. Claims 1-30 are presented for examination.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1, 11 and 21 are rejected under 35 U.S.C. 102(a) as being anticipated by Brown (U.S. Patent 6,128,308, hereinafter Brown).

Per claims 1, 11, and 21, Brown teaches:

a task table coupled to a bus interface to store task entries corresponding to tasks executed by at least one processor (col. 2, lines 65-68, continued on col. 3, lines 1-11, **The DFP provides an interface between the MCU, the DSP, and the memory, and later a task list to the memory which comprises tasks to be executed by the DSP. The DSP executes the tasks in the task list, and for bus interface,** additionally col. 3, lines 66-68, continued on col. 4, lines 1-2, **The first memory bus couples the memory to the DFP and the second memory bus couples the memory to the DS-P);**

a block allocation circuit coupled to the bus interface and a cache memory to allocate blocks of the cache memory used by at least one of the tasks (**memory management: when data buffers & data streams for each task should be allocated,** col. 10, lines 7-8); and

a task coordinator to coordinate the tasks in response to a task cycle issued by the at least one processor (**DSP's 300 executive routine (EXEC) will perform management of the task list using the data streams,** col. 14, lines 7-17, and for the cycle of processor see, col. 10, lines 66-

Art Unit: 2127

68, continued on col. 11, lines 1-10, **the timer block and W/R cycle through DFP 320, and FIG.3).**

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 2-3, 12-13, and 22-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (U.S. Patent 6,128,308, hereinafter Brown) in view of Tuma et al. (U.S. Patent 6,173,385, hereinafter Tuma).

Per claims 2-3, the reference of Brown while teaches of the task identifier or task ID (col. 10, lines 5-6, Fig 23, **Task List Table, task #**), task address and task cache address (col. 8, lines 29-35, RAM memory address), and task block size (col. 25, lines 40-54, **buffer address and buffer block size**), fails to teach of task start address. However, finding the start address of a task is notoriously well known in the art as it is evidenced by Tuma et al. The reference of Tuma teaches of finding the start address (col. 4, lines 9-25, by clocking each of these counters. The 24 bit output signal of counters U6, . . . ,U11 are provided to the memory array as the **starting address for reading or writing** this particular logical block) for the purpose of being able to Read/Write of the logical block). Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to modify the system of Brown to show the start of the

Art Unit: 2127

memory address to make the system more efficient by preventing fragmented areas of memory.

5. Claims 4-10, 14-20, and 24-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (U.S. Patent 6,128,308, hereinafter Brown) in view of Tuma et al. (U.S. Patent 6,173,385, hereinafter Tuma), and further in view of Nagata (U.S. Patent 5,138,696, hereinafter Nagata).

Per claims 4, 14, and 24, use of the busy flag to show the block of memory is free or in use is well known in the art as it is evidenced by Nagata (see Nagata, col. 4, lines 10-45, See a free block retrieve table), for the reason to be able to use the blocks of memory after the block is used and freed. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to indicate the status of memory as to whether it is busy or freed and make the system more efficient as far as memory use.

Per claims 5-6, 15-16, and 25-26, task table status updating is well known in the art (See, Brown, Fig. 24, the Update Buffer Status and all the other task statuses).

Per claims 7, 17, and 27, see Brown Fig. 23.

Per claims 8-10, 18-20, and 28-30, See Brown col. 19, lines 39-56, for lines memory mapping, block size, cache lines RAM, and registers, and col. 17, lines 13-18 for Internal/External memory functions.

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Art Unit: 2127

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Majid A. Banankhah** whose voice telephone number is **(703) 308-6903**. A voice mail service is also available at this number.

All response sent to U.S. Mail should be mailed to:

Commissioner of Patent and Trademarks

Washington, D.C. 20231

Hand-delivered responses should be brought to Crystal Park Two, 2021 Crystal Drive, Arlington, VA, Six Floor (Receptionist). All hand-delivered responses will be handled and entered by the docketing personnel. Please do not hand deliver responses to the Examiner.

All Formal or Official Faxes must be signed and sent to either (703) 308-9051 or (703) 308-9052. Official faxes will be handled and entered by the docketing personnel. The date of entry will correspond to the actual FAX reception date unless that date is a Saturday, Sunday, or a Federal Holiday within the District of Columbia, in which case the official date of receipt will be the next business day. The application file will be promptly forwarded to the Examiner unless the application file must be sent to another area of the office, e.g., Finance Division for fee charging, etc.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is **(703) 305-9600**.

Majid Banankhah

11/17/03


MAJID A. BANANKHAH
PRIMARY EXAMINER